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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,163	05/01/2001	Tatsuru Namatame	15.43/5851	5642

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EXAMINER	
FOONG, SUK SAN	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/847,163	Applicant(s) NAMATAME ET AL.	
	Examiner Suk-San Foong	Art Unit 2823	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *17-20* is/are withdrawn from consideration.

5)☒ Claim(s) *16,21-26 and 30* is/are allowed.

6)☒ Claim(s) *6-15 and 27-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 11 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 9-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no description in the specification as originally filed of forming a protection film prior to forming an anti-oxidation film as opposed to forming anti-oxidation film 82 then forming protection film 90 (instant p. 9, line 9, to p. 12, line 5). (See MPEP 2163).

3. Claims 28 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 28, line 9, it appears that the term--nitride--should be inserted after "oxide".

Claim Rejections - 35 USC § 103

5. Claims 6, 7, 13, 14, 15 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruo ('090) in combination with Mizutani ('128).

Maruo teaches a method of forming high breakdown voltage CMOS transistors which includes forming silicon oxide film 14' over silicon substrate 10 (Col. 7, line 60-62, and Fig. 3B), then forming silicon nitride film over substrate 10 (Col. 7, lines 63-64), etching silicon nitride film 26 to expose portions of substrate 10 that are not in element forming regions (Col. 7, lines 64-65, and Fig. 3C), then applying photoresist 27 over substrate 10 and providing openings at LOCOS forming regions (Col. 7, line 66 to Col. 8, line 1), subsequently implanting impurity at the openings of first and second LOCOS regions to form first and second offset impurity layer 17 (Col. 8, lines 1-6, and Fig. 3C), then applying and patterning photoresist 27 to form channel stopper regions 12 at the openings of a third LOCOS region by ion implantation (Col. 8, lines 7-15, and Fig. 3D), then performing wet oxidation at 950°C to form first and second LOCOS oxide layer 15 and third LOCOS oxide layer 11 wherein first and second offset impurity layers 17 are below LOCOS layers 15 (Col. 8, lines 16-20, and Fig. 3E), then growing gate dielectric layer 14'' after removing silicon nitride layer 26 and oxide layer 14' from substrate 10 (Col. 8, lines 23-27, and Fig. 3F), subsequently forming gate electrodes 16 and 20 in between LOCOS oxide layers 11 and 15 (Col. 8, lines 38-44, and Fig. 3F), and then forming source and drain regions 18 and 18a such that first LOCOS oxide layer 15 is between gate dielectric layer 14'' and drain region 18, and second LOCOS oxide layer 15 is between gate dielectric layer 14'' and source region 18a (Col. 9, lines 11-16, and Fig. 3I).

Maruo does not teach forming first and second recessed sections where LOCOS layers are to be formed.

Mizutani teaches a method of forming a semiconductor device which includes forming a buffer oxide film over substrate 50, then forming anti-oxidation layer 52 such as silicon nitride over a buffer oxide film (Col. 4, lines 16-19), subsequently forming a first and second recessed sections in substrate 50 with a tapered angle of 60° (Col. 4, lines 19-27 and Fig. 4A), then forming subsequently implanting an impurity into the first and second recessed sections (Col. 4, lines 31-36 and Fig. 4C), and then performing a thermal oxidation process to form the first LOCOS layer 60 in the first section and the second LOCOS layer 60 in the second section by using anti-oxidation layer 52 as a mask (Col. 4, lines 57-64, and Fig. 4D).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Maruo with Mizutani because it would enable formation of LOCOS oxide layers 11 and 15 of Maruo to be performed.

Examiner takes official notice that thermal oxidation step includes performing heat treatment in an atmosphere containing oxygen were known at the time of applications invention.

It would have been within the scope to one ordinary skill in the art to combine the combination process with the known process because it would enable formation of the LOCOS layers of the combination process to be performed.

In regard to claim 27, the step recited in lines 22-28 would be obtained as the same materials are being treated the same as the instant invention.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maruo ('090) in combination with Mizutani ('128) as applied to claims 6, 7, 13, 14, 15, 21 and 24-27 above.

The choice of thickness of anti-oxidation layer would have been a matter of routine optimization to achieve the desired device densities and the desired device characteristics to be formed. (See MPEP 2144.05).

7. Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruo ('090) in combination with Mizutani ('128) as applied to claims 6, 7, 13, 14, 15 and 27 above, and further in view of Iyer et al. ('631).

The combination process does not disclose forming a silicon oxide nitride layer over silicon substrate.

Iyer et al. discloses a method of forming isolation regions for integrated circuites which includes forming ARC layer 306 such as silicon oxynitride (silicon oxide nitride) over silcon substrate 300 (Col. 9, lines 29-32, and Fig. 3A), then forming silicon nitride layer 201 over ARC layer 306 (Col. 9, lines 40-42, and Fig. 3B), and then forming LOCOS layer 322 (Col. 10, lines 8-9, and Fig. 3E).

It would have been within the scope to one ordinary skill in the art to combine the teachings of the combination process with Iyer et al. because it would enable formation of the LOCOS layer of the combination process to be performed.

Response to Arguments

8. Applicant's arguments with respect to claim 6 and claims dependent thereon have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

9. Claims 16, 21-26 and 30 are allowed.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suk-San Foong whose telephone number is 703-305-0383. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 (7724, 3431, 3432).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

GV
May 18, 2003

George Fourson
Primary Examiner
Art Unit 2823